Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **D0**
2. **D1**
3. **D2**
4. **D3**
5. **VEE**
6. **NOT Q**
7. **Q**
8. **VCC**

**.041”**

**1 8**

**7**

**6**

**2**

**3**

**4 5**

**KL32**

**AC76**

**MASK**

**REF**

**.041”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: KL32 / AC76**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 4/23/19**

**MFG: ON SEMI THICKNESS .008” P/N: MC100EL01**

**DG 10.1.2**

#### Rev B, 7/19/02